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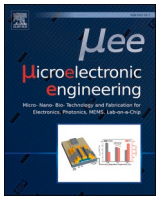

Electrical characterization of flexible hafnium oxide capacitors on deformable softening polymer substrate

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ABSTRACT

In this work, we investigate the electrical performance and compatibility of low-temperature hafnium oxide (HfO_2) thin-film capacitors on a novel softening polymer substrate. Metal-insulator-metal HfO_2 capacitors were fabricated using HfO_2 as the dielectric material, deposited at 100 °C by atomic layer deposition (ALD), and gold as the top and bottom contacts. The HfO_2 capacitors were fabricated on silicon and on softening polymer substrates with a dielectric thickness of 50, 40, 30, and 20 nm. The electrical performance of the MIM capacitors was measured and compared to determine the quality and compatibility of the low-temperature HfO_2 deposition with the silicon and polymer substrate. The dielectric constant varied from 12 to 17 as the HfO_2 thickness increased from 20 to 50 nm. Moreover, the capacitance density and dielectric constant of the capacitors on the polymer substrate differed by 3.9% ± 2% and 3.4% ± 2% with respect to the silicon substrate. The polymer substrate devices also have a higher leakage current, which suggests a higher number of defects in the dielectric film relative to Si substrates. Finally, the devices on the polymer substrate were subjected to bending cycles (up to 10^5 cycles) with a 5 mm bending radius to evaluate the resilience of the HfO_2 capacitors against mechanical stress. The results show that the fabrication of the HfO_2 thin-film capacitors on the softening polymer substrate is achievable with high stability and mechanical resilience. Overall, this research could assist the production of flexible biomedical devices on softening polymer substrates.

1. Introduction

Recent developments in new flexible materials and semiconductors compatible with microfabrication processes are propelled by a growing interest in applications for flexible electronic technologies, including solar cells, RF antennas, and biomedical devices [1–4]. Utilizing thin-film semiconductor process technology has helped overcome many limitations and problems in the field of electronic flexible devices. However, migrating active circuits from rigid silicon (Si) wafers to soft and flexible substrates is a challenge that has limited the widespread implementation of flexible electronics technology. Even though studies of electronic components such as thin-film transistors (TFTs), diodes, and capacitors on flexible substrates have shown the feasibility of flexible technologies [5–13], there still are some unexplored topics that are just as important in the development of flexible devices. In this case, the quality of high-k gate dielectrics is one of the topics often overlooked, yet significant for flexible electronics [14–16]. For years, high-k dielectrics have been used on rigid substrates, like Si or glass, as insulators between the gate contact and the active channel of a TFT to reduce the gate current and improve the electrical performance of TFTs [17–20]. Notably, the use of hafnium-based high-k dielectrics has been highlighted in this field because of its wide bandgap, high dielectric constant, and thermal stability [21–25]. However, when a high-k dielectric is deposited on a flexible polymeric substrate, the electrical properties of the dielectric are affected by the low-temperature, low-stress process limitations, and overall mechanical characteristics of the polymer substrate. Unlike Si wafers, polymeric substrates are limited to low temperatures (<600 °C), such as polyimide, which has a thermal

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degradation temperature of ~580 °C [26,27]. Additionally, high-k dielectrics, as well as the subsequential layers deposited on the substrate, can experience mechanical stress from expansion/contraction cycles during the fabrication process which can lead to, delamination before fabrication is completed. These dimensional changes generate imperfections, stress, or fissures in the dielectric film that often significantly affect the electrical performance of TFTs.

As previously reported, thiol-ene/acrylate polymers have been used as a substrate for the development of passive biomedical devices such as spinal cord stimulators and nerve cuffs [28–30], due to their deformable and softening properties. This polymer, also known as a shape memory polymer (SMP) because of its mechanical properties [31,32], has demonstrated compatibility with standard semiconductor fabrication processes, resilience to temperatures up to 350 °C without any significant degradation, and dimensional stability during fabrication [26,33–35]. Furthermore, the biocompatibility of the polymer and its ability to soften by reducing the storage modulus three orders of magnitude from GPa to MPa, and increase the strain capacity from 10% (dry) up to 250% in physiological conditions, can enable the fabrication of biomedical devices with active components, which could benefit the long-term implantation of these type of devices [26,36–38].

In this work, the high-k dielectric hafnium oxide (HfO_2) is used as an insulator in metal-insulator-metal (MIM) capacitors on Si and SMP substrates. The HfO_2 capacitors were electrically characterized to evaluate the quality of the HfO_2 film and the compatibility of the low-temperature deposition process when using a rigid or flexible substrate. By characterizing and comparing the electrical properties of both films, a better understanding of low-temperature deposition methods of high-k dielectrics for flexible electronics is presented. We focus on the electrical properties of the HfO_2 dielectric layer deposited at a low temperature (100 °C) on the SMP substrate, where the behavior of the capacitance density, dielectric constant, and leakage current of HfO_2 MIM capacitors with 4 different dielectric thicknesses was analyzed. Furthermore, a mechanical bending study was performed to investigate the effects of mechanical stress on the electrical properties and performance of the HfO_2 capacitors and determine their resilience to multiple bending cycles (up to 10^5 cycles). This contribution to the field of flexible electronics could assist with the understanding and development of active electronic circuits on flexible, softening materials for bioengineering applications.

2. Experimental

For this study, we fabricated meta-insulator-metal (MIM) HfO_2 thin-film capacitors using two types of substrates: silicon (Si devices) and thiol-ene/acrylate-based shape memory polymer (SMP devices). The Si substrate was prepared with 1 μm of thermal growth SiO_2 layer for insulation and served as the control. The SMP substrate was synthesized from the following monomers and photo-initiator: 1, 3, 5-Triallyl-1, 3, 5-triazine-2, 4, 6(1H, 3H, 5H)-trione (TATATO), Tricyclo [5.2.1.02, 6] decanedimethanol-diacrylate (TCMDA), Tris [2-(mercaptopropionyloxy) ethyl] isocyanurate (TMICN), and 2, 2-Dimethoxy-2-phenyl-acetophenone (DMPA) as photo-initiator (PI). The monomer mixture was prepared in a 20 mL glass vial and mixed using a dual asymmetric centrifugal speed mixer. Additionally, throughout the process, the monomer mixture was protected from light exposure to avoid premature polymerization. The solution was spin-coated on a 2″ x 3″ glass slide at 650 rpm with an acceleration of 100 rpm/s for 60 s to obtain a 50 μm layer. Then, the spin-coated layer was exposed to 254 nm UV-light for 2 min to initiate polymerization and subsequently for one hour in a 365 nm UV-light. Finally, the thiol-ene/acrylate substrate on glass was transferred into a vacuum oven at 120 °C for a day to further crosslink the polymer, reduce moisture, and remove residue monomers.

Both types of samples were fabricated simultaneously in a 10,000-class clean room, using standard semiconductor and photolithography processes. First, a 200 nm gold (Au) layer was deposited by electron beam evaporation on top of the Si and SMP substrates at a deposition rate of <1.5 Å/s to keep a uniform layer and etched with potassium iodide solution to pattern the bottom contact. The Si samples have an additional chrome (Cr) layer of 20 nm between the Au and the thermal SiO_2 working as an adhesion layer. Then, the HfO_2 dielectric layer was deposited by atomic layer deposition (ALD) at 100 °C varying the cycles to obtained different thicknesses (50, 40, 30, and 20 nm), and patterned with buffered oxide etch (BOE) 7:1. The precursors used in this deposition were a tetrakis(dimethylamido) precursor for hafnium with a pulse time of 0.4 s and a wait time of 8 s and deionized water (DIW) for oxidation with a pulse of 0.015 s and wait time of 10 s. The number of cycles utilized for each thickness was 365 cycles for 50 nm, 292 cycles for 40 nm, 219 cycles for 30 nm, and 146 cycles for 20 nm. After the deposition, the thickness of each sample was measured by ellipsometry from silicon samples with 1 μm of SiO_2 thermally growth. To complete the devices, a second Au layer of 200 nm was deposited and etched with the same procedure as the bottom contact to pattern the top contact. Finally, we exposed all the devices to an annealing treatment at 200 °C in an oxygen (O_2) atmosphere for 2 h. Fig. 1a and b show the top view of the capacitors on Si and SMP, respectively. Both types of devices (Si and SMP) have capacitors of different areas (1×10^{-4}, $2 \times 10^{-4,}$ and 4×10^{-4} cm^2) to track the proportional behavior of the capacitance as a function of the area and obtain an accurate average value of capacitance density, dielectric constant, and leakage current density. For each substrate, we measured a total of 48 capacitors that are divided into 12 from each thickness and 4 from each area. Then, the SMP devices with the 50 and 20 nm dielectric layer were encapsulated with a second layer of SMP (5 μm). Additional photolithographic steps were employed to access the capacitor's contacts. Finally, the encapsulated capacitors were cut into strips of 1″ x 2″ and released from the glass carriers by immersing them in deionized water for 24 h and then dried at room temperature for 3 days. The released devices are illustrated in Fig. 1c and d. After this process, we exposed the released devices to a bending fatigue test. The capacitors were fixed to a mobile fixture of a homemade bending machine and bent in compression for sets of 10^2, 10^3, 10^4, and 10^5 cycles with a 5 mm bending radius. The fixture moved from the rest position (30 mm from the base) to the bending position at a frequency of 1 Hz. The electrical characterization of the capacitors was carried out at different steps of the experiment: after the fabrication, the posterior thermal treatment, and each bending set (released devices). The completed devices were measured using a Cascade-Microtech® probe-station model Summit 12000B-M with a semiconductor analyzer Keithley 4200 and HP/Agilent 4284A Precision LCR Meter to obtain the capacitance density, dielectric constant, and leakage current.

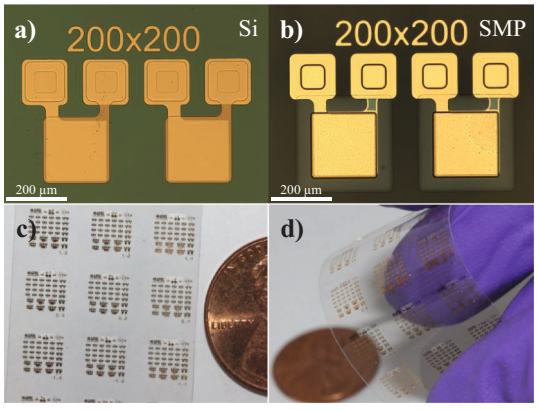

Fig. 1. Top view of HfO2 capacitors (4 × 10–4 cm2) fabricated on a) Si and b) SMP substrates. Optical images of the fabricated capacitors on the SMP substrate c) released, and d) bent.

3. Results and discussion

In order to determine the compatibility of the SMP substrate with the HfO_2 film deposited at low temperature, the electrical performance of the capacitors on Si and SMP were compared. Fig. 2a and b display the capacitance density of the HfO_2 devices with overlaid thicknesses on Si and SMP as a function of frequency from 1 kHz to 10 MHz with an applied voltage of 5 V. In both substrates, the capacitance is static for all four different thicknesses from 1 kHz to 1 MHz. For the Si substrate, the average capacitance density for the 20 and 50 nm HfO_2 layers obtained between 1 kHz and 1 MHz was 0.59 and 0.30 μF/cm^2, respectively. Similarly, the SMP substrate demonstrated a capacitance density of 0.56 and 0.32 μF/cm^2 for the 20 and 50 nm HfO_2 layers. The inset in both charts displays the dielectric constant of each thickness measured from −5 to 5 V at 1 MHz. The dielectric constant was obtained from the measurement of the capacitance and calculated using the equation $C_{ox} = \frac{\varepsilon_0 k}{t}$, where $\mathbf{C_{ox}}$ is the capacitance density measured from the 96 capacitors in this study (48 for each substrate), $\boldsymbol{k}$ the dielectric constant, $\boldsymbol{\varepsilon_0}$ the vacuum permittivity, and $\boldsymbol{t}$ the dielectric thickness measured (50, 40, 30, and 20 nm). The HfO_2 capacitors with the 50 nm thick layer showed the highest dielectric constant at ~17 for the capacitors fabricated on Si and ~ 16 for the capacitors on SMP, while the lowest dielectric constant values came from the 20 nm HfO_2 capacitors with the dielectric constant values of ~13 and ~12, for Si and SMP, respectively. Generally speaking, the dielectric constant is independent of thickness and should remain constant when the thickness is modified. However, this is not the case since in both types of substrates the dielectric constant decreases as the HfO_2 thickness decreases. This behavior could be associated with the dielectric constant in the Au-HfO_2 interface, which is affected by the Au-HfO_2 interactions during the growth of the first nanometers of the film and degrades the effective dielectric constant [39–41]. Fig. 2c and d display the leakage current density (A/cm^2) as a function of the electric field up to 1 MV/cm of 96 newly fabricated non-stressed capacitors (48 on each substrate and 4 for each area). In both substrates, the leakage current remains below 0.1 μA/cm^2 when reaching 1 MV/cm. In the case of the Si devices, the current stays constant for all different thicknesses, which suggests a similar layer quality among the capacitors. On the other hand, the SMP devices exhibit a slight increase in the leakage current, indicating an increase of defects and therefore a decrease in the quality of the HfO_2. The insets in both charts (Fig. 2c and d) show the leakage current of the four different films, as the electric field is increased from 0 to 10 MV/cm. Here, we observe the dielectric breakdown of the four HfO_2 films of each substrate, where a dielectric strength (E_{br}) above 6 MV/cm is required to break the dielectric film.

The values of the leakage current at 1 MV/cm, capacitance density, and dielectric constant at 1 MHz were selected from the data plotted in Fig. 2 and compared in Fig. 3. The relationship between leakage current and dielectric thickness of the HfO_2 capacitors at 1 MV/cm is shown in Fig. 3a. Ideally, the leakage current should be the same under the same electric field at 1MV/cm, however, two trends are observed. First, the leakage current of both substrates increases as the insulator thickness decreases, and second, the SMP capacitors present a higher leakage current than the capacitors fabricated on Si. The first trend can be related to bulk and Au-HfO_2 interface defects. Since gold is one of the least reactive chemical elements, the first atomic layers of HfO_2 contain a higher amount of imperfections that become insignificant with the increase of thickness. This Au-HfO_2 interface has been studied using different photoelectron spectroscopy techniques, where the Au atoms showed poor or no interaction with oxides layers [42–46]. As a result, the Au-HfO_2 interface for the 20 nm HfO_2 capacitors plays a larger role compared to the 50 nm HfO_2 capacitors. For the second trend, we need to consider the response of the SMP substrate to the temperature cycles during the fabrication process. The temperature changes during fabrication expand and contract the SMP substrate, which generates mechanical stress on the dielectric film and likely increases the number of imperfections. These imperfections increase the number of leakage pathways available and therefore a higher leakage current is presented

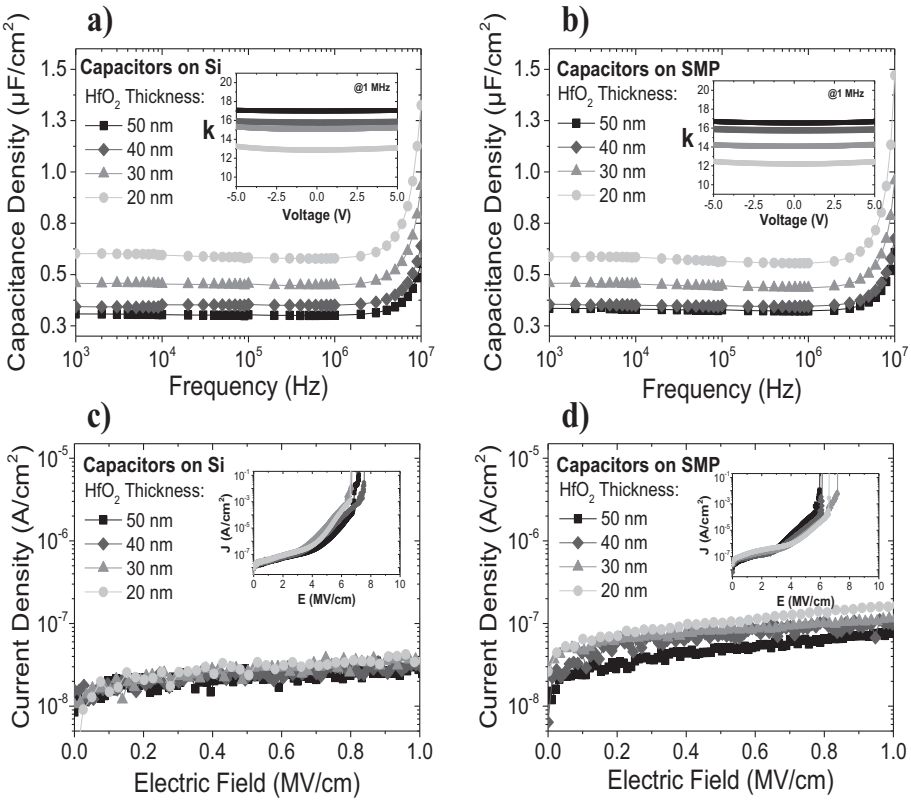

Fig. 2. The capacitance density of the MIM capacitors fabricated on a) Si and b) SMP substrates with 50, 40, 30 and 20 nm of HfO2 dielectric film, as a function of frequency. In both insets is illustrated the dielectric constant of the different dielectric thicknesses calculated from C—V measurements, as a function of voltage. The leakage current density of the MIM capacitors fabricated on c) Si and d) SMP with 50, 40, 30 and 20 nm of HfO2 dielectric film, as a function of electric field. The insets present the dielectric breakdown of the four different dielectric thickness.

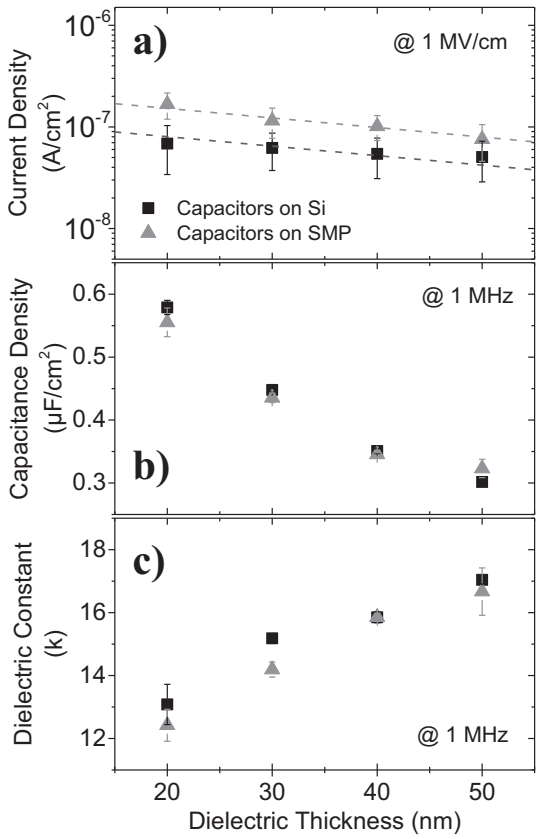

Fig. 3. a) The leakage current density b) capacitance density and c) dielectric constant vs the dielectric thickness of the HfO2 capacitors fabricated on Si and SMP substrates. The leakage current density was measured at 1 MV/cm. Capacitance density and dielectric constant were measured with an AC overlaid signal at 1 MHz.

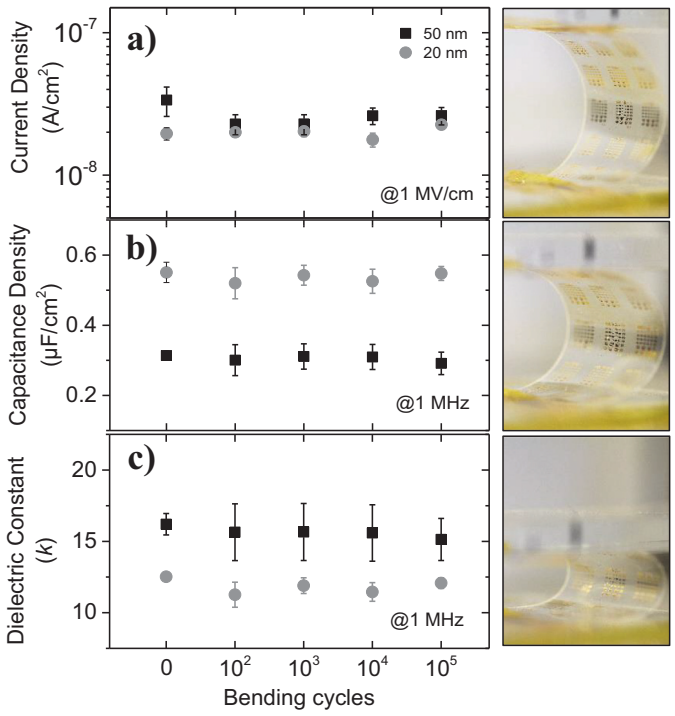

Fig. 4. a) The leakage current density, b) capacitance density and c) dielectric constant of the HfO2 capacitors with 50 and 20 nm fabricated on SMP as a function of bending cycles with a bending radius of 5 mm in compression. The inset pictures show the progression of the device strip from a relaxed to a compressed position.

in the devices on the polymer substrate. Fig. 3b and c present the capacitance density and dielectric constant at 1 MHz of the Si and SMP devices as a function of the dielectric thickness. In the case of the capacitance density (Fig. 3b), both types of substrates gave similar measurements with a 3.9% ± 2% of change between the Si and SMP devices. Similarly, the dielectric constant (Fig. 3c) of both substrates shows a reduction of the dielectric constant of 3.4% ± 2% of the capacitors on SMP. However, capacitors on both substrates show degradation as seen by the decrease in the dielectric constant and becoming more pronounced as the HfO_2 thickness decreases. This behavior agrees with the statement mentioned previously in Fig. 2, where the generation of imperfections in the Au-HfO_2 interface degrades the effective dielectric constant and becomes insignificant with the increase of the dielectric thickness [39–41]. With this information we can conclude that the capacitors perform similarly in both the Si and SMP substrate, low-temperature fabrication processes for HfO_2 are compatible with the SMP substrate, and the quality of the HfO_2 film is dependent on the thickness of the film.

To test the mechanical resilience and electrical stability of the HfO_2 film on the SMP substrate, we performed a bending fatigue test on the 50 and 20 nm capacitors with a bending radius of 5 mm. The capacitance density at 1 MHz and leakage current at 1 MV/cm of nine capacitors (3 for each area) from each thickness was measured after 10^2, 10^3, 10^4, and 10^5 bending cycles as shown in Fig. 4. In this test, the leakage current for the capacitors with 50 and 20 nm of HfO_2 decreases after being released from the glass carrier. Then, after the bending cycles, the leakage current stabilizes within the 10^{-8} A/cm^2 range, as displayed in Fig. 4a. Furthermore, the capacitance density (Fig. 4b) shows a similar behavior during the bending test, which changes from 0.31 to 0.29 μF/cm^2 and 0.55 to 0.52 μF/cm^2 for the 50 and 20 nm devices, respectively. Finally, Fig. 4c presents the dielectric constant of the 50 and 20 nm capacitors at 1 MHz, which was calculated from the capacitance density measured for the bending test. In this case, the dielectric constant shows a steady behavior as the bending cycles increase. For the 50 nm devices, the dielectric constant varies between 16 and 15, and between 12 and 11 for the 20 nm capacitors. Overall, the 50 and 20 nm HfO_2 films demonstrate a stable electrical performance and mechanical resilience, even though the leakage current decreases significantly. This increase in current could be explained by the water diffusion while the SMP devices were immersed in deionized water for 24 h. Although the capacitors were encapsulated with a 5 μm SMP layer, this polymer has a water absorption of ≈3% that can affect the gold traces or the Au-HfO_2 interface [47,48]. However, it is important to mention that to get a more detailed lifetime span and tolerance of these types of devices; further mechanical studies are required with a higher number of bending cycles and smaller bending radius.

4. Conclusion

In this work, we investigated the quality and compatibility of low-temperature deposited HfO_2 films on a softening polymer substrate. The MIM HfO_2 capacitors were fabricated on Si and SMP substrates and the electrical properties of the HfO_2 films were compared. The results exhibited similar electrical performance between the Si and SMP devices, where the capacitance density and dielectric constant of the SMP capacitors vary approximately 3% from the Si-based devices. On the other hand, the SMP capacitors showed a higher leakage current that could be associated with the expansion and contraction of the polymer substrate during the fabrication. Additionally, we observed that in both types of capacitors (Si and SMP devices), the dielectric constant tends to decrease as the thickness of the HfO_2 film decreases. On the other hand, the leakage current increases as the dielectric thickness decreases. These two behaviors could be related to the imperfections in the Au-HfO_2

interface, which degrade the quality of the film. Finally, bending fatigue tests demonstrate the resilience and stability of the HfO_2 film on SMP after 10^5 cycles. The results presented in this work could assist in the development of flexible active circuits and pave the way towards the fabrication of flexible and active biomedical devices.

Credit Author Statement

Ovidio Rodriguez-Lopez: Fabrication of thin-film devices, electrical characterization, data analysis, and document writing (original).

Alexander J. Polednik: Electrical characterization, investigation, and documentation.

Adriana C. Duran-Martinez: Material characterization (thickness, roughness), and document writing.

Aldo Garcia-Sandoval: Mechanical and electrical characterization, data analysis, and writing (review and editing).

Edgar Guerrero Ruiz: Fabrication process definition, investigation, and writing (review and editing).

Walter Voit: Funding, supervision, and conceptualization.

Gerardo Gutierrez-Heredia: Structure designs, fabrication process definition, data analysis, and writing (original, review and editing).

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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