A Systematic Study on BEOL Defectivity Control for Future AI Application

James H.-C. Chen, Fee li Lie, Scott DeVries, Carol Boye, Sanjay Mehta, Thamarai S. Devarajan, Mary-Claire Silvestre, Wei-Tsu Tseng, and Massud A Aminpur

IBM Research, 257 Fuller Road, NFE Suite 3100, Albany, New York 12203, USA

E-Mail: jhchen@us.ibm.com

***Abstract*—In this paper, a case study on control of BEOL defectivity in a systematic way for the future AI application is presented. A few novel methodologies were introduced to identify the source of defectivity in various BEOL sectors, such as, patterning, barrier deposition, plating, and CMP. We successfully reduced the defectivity to the level required to yield target AI devices.**

Keywords—BEOL, defectivity control, AI application

I. Introduction

In order to achieve future high-speed and low power consumption AI devices, a robust and low defectivity process is critical [1-2]. In order to achieve a high yield large scale artificial neural network, defectivity of patterning, metallization, and CMP is important, because the large numbers of layer in BEOL. However, the conventional approach of yield improvements are time and resource consuming. As a result, innovative methodologies are necessary. In this paper, a systematic study with innovative methodologies are presented for a robust BEOL process to the future AI application.

II. Experimental

A 14 nm node vehicle with a 17 m long comb-serp and a 19.6 M via chain macro were introduced in a 300 mm production line for this study. A bright field defect inspection tool was used to monitor the defectivity post lithography, RIE, copper barrier/seed, and CMP.

In order to understand the relationship of plating edge bevel removal (EBR) to etch behavior, three EBR widths from -1.8 mm, -0.2 mm, to 0.3 mm with respect to lithography edge bead removal (EBR) were conducted. The minus conditions will leave a copper ring on the wafer. It will be exposed in the etch of next metal level. The exposed copper may change the etch chamber behavior.

In order to understand the particle performance in the copper barrier/seed process, a few innovative methodologies were introduced. Firstly, an un-patterned wafer, which skips the lithography step, was used to test the particle performance of the PVD system. Secondly, another un-patterned wafer with regular wet clean went through the same test. Then, a third un-patterned wafer with regular etch and wet clean was used for the same test for comparison. As a result, the particle performance with respect to lithography, etch, and wet clean, could be deconvoluted by this methodology.

III. Discussion

The major defectivity in each module will be shown and the approaches to reduce it will be presented.

Etch optimization

The major yield detractor post etch found by the bright field defect inspection tool is a hair-like defect, as shown in Fig. 1. They were initiated at the corner of the pattern and spread out along the edge. This is also an indication of weakness point of the process where the etch stop layer was punched through. In Fig. 2, EDX elementary analysis showing the hair-like defect has strong copper signal. This is an evidence of exposure of copper underneath and it might poison the etch chamber.

In Fig. 3, an example was showing the RIE defects found in the via chain area. This copper-polymer does degrade the electrical yield.

Based on this finding, a linear relationship between electrical yield to physical limited yield can be derived as shown in Fig. 4 and 5 by a data fitting. As a result, the yield detractors can be realized. Thus, a novel methodology of RIE process optimization is established with this correlation.

Particle control at the bevel

Spike in particle counts has been observed in the degas chamber of the PVD system used for liner deposition prior

to Cu plating. In order to quickly partition the possible source of the particle increase, blanket wafers were used and then ran through degas chamber only. As mentioned, blanket wafers post deposition and post dielectric etch and clean were ran through the degas chamber. Pre and post particle count were recorded during the runs. Particle count shown in Fig. 6, indicates that after POR wafers run (points A, B, D), the wafer count would spike higher. Point E which is also a POR wafer but a different product didn't show any increase in particle count. For the blanket wafer run post dielectric deposition (point C) particle count level did not increase. However, for blanket wafer that ran through etch and clean (point F) the particle count increased beyond the spec limits. EDX on the particles in the degas chamber showed strong C-F signal as shown in Fig. 7. Baseline brightfield inspection post dielectric etch doesn't show particle as one of the defects of interest so inspection at the bevel was used to determine possible source for this particle. Partition SEM cut on patterned wafer revealed that post dielectric etch, prior to clean, a thick residue is formed at the bevel backside as shown in Fig. 8. SEM cuts around the bevel confirms this RIE residue extended to 0.1-0.2 mm of the backside, as shown in Fig. 9. EDX analysis identifies this residue is composed of C-F elements as shown in Fig. 10. By introducing a short N2/H2 post etch treatment (PET) and a purge step pre and post degas, the particle spike at the degas chamber has been reduced to acceptable levels as seen in Fig. 11. Long term, a bevel backside clean or optimization of etch recipe to remove the residue at the bevel backside is needed.

Plating edge bevel removal and etch behavior

We discovered the edge copper ring will decrease the dielectric etch rate and cause roughness on the dielectric surface. As a result, a unique methodology was developed to optimize the number of plating edge bevel removal (EBR). Fig. 12 is the process emulation showing the major process steps in this study. A full wafer CD measurement map was used to monitor the etch rate and surface roughness at edge chips vs plating EBR, as shown in Fig. 13. In Fig. 13, the normalized etch rate of wafer edge to the center was plotted against the difference of plating EBR to litho EBR are plotted. The data are showing a linear relationship to the width of copper ring. A wider copper ring will yield a lower dielectric etch rate and cause a rough dielectric surface. As a result, optimized plating EBR helps to increase the utilization of the wafer.

Copper CMP optimization:

We compared the solid content of two slurries from 11.5% to 2 %, respectively, to fine tune the polishing scratches. Fig. 14 is showing the scratches trend chart against the solid contain of barrier slurries. The polish scratches are found to be a function of the solid content.

IV. CONCLUSION

In summary, a meaningful correlation between physical limited yield and electrical yield are obtained in this study. This is a good demonstrate how to evaluate how successful of the defect reduction. This will enable insertion of future AI devices into a healthy and robust BEOL baseline.

ACKNOWLEDGMENT

This work was performed by the research alliance teams at various IBM research and development facilities.

REFERENCES

[1] Ghalia Tello, Omar Y. Al-Jarrah, et al., "Deep-Structured Machine Learning Model for the Recognition of Mixed-Defect Patterns in Semiconductor Fabrication Processes", *IEEE Transactions on Semiconductor Manufacturing*, pp. 315-322, Vol. 31, Issue 2, May 2018. DOI: 10.1109/TSM.2018.2825482.

[2] Fatima Adly, Paul D. Yoo, et al., "Randomized General Regression Network for Identification of Defect Patterns in Semoconductor Wafer Maps", *IEEE Transactions on Semiconductor Manufacturing*, pp. 145-152, Vol. 28, Issue 2, May 2015. DOI: 10.1109 /TSM.2015.2405252

[3] Eswar Ramanathan, Antonio Fiacco, et al., "A Study on the Interaction between Barrier and Plating Causing Edge Stringer Defects in 28nm", Proc. of ASMC, pp. 79-82, 2016.

[4] Balajee Rajagopalan, Jean-Baptiste Laloe, et al., "Extra-pattern Killer Defectivity Improvement and Enhancement of within-feature Barrier coverage by Optimization of TaN Barrier PVD process in 90p Cu wire interconnects for 28 nm Technology", Proc. of ASMC, pp. 354-357, 2016.

[5] Mary Claire Silvestre, Eswar Ramanathan, et al., "Bevel Rinse Optimization for Reduced Edge Defectivity and Improved Edge Yield", Proc. of ASMC, pp. 124-128, 2016.

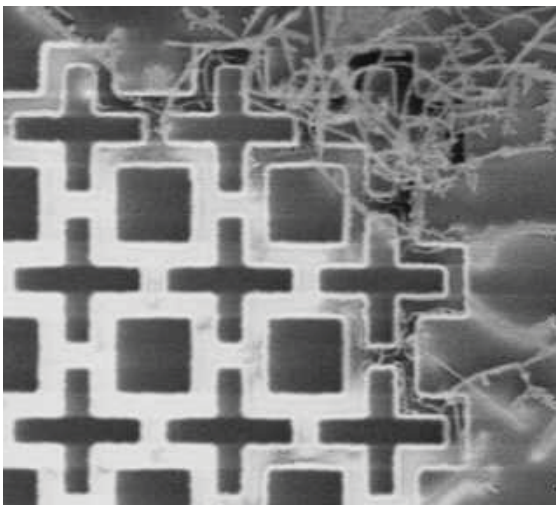


Fig. 1 A hair-like defect found by bright field inspection tool. It is also an indication of weakness point of the process.

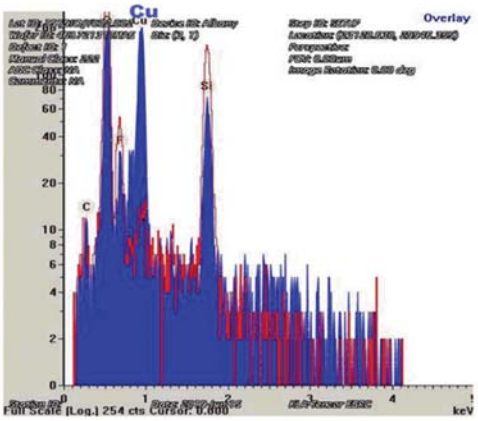


Fig. 2 EDX elementary analysis showing the hair-like defect has strong copper signal. This is an evidence of exposure of copper underneath.

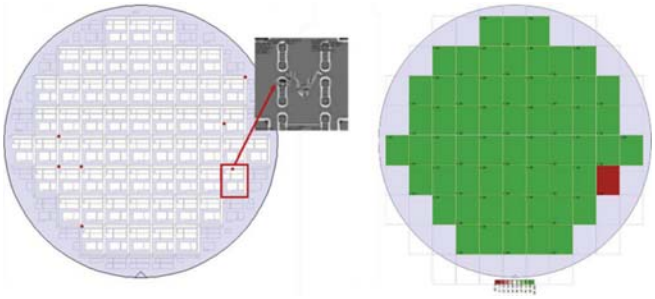


Fig. 3 Example showing how the copper-polymer defect degrading the electrical yield at a large via chain macro.

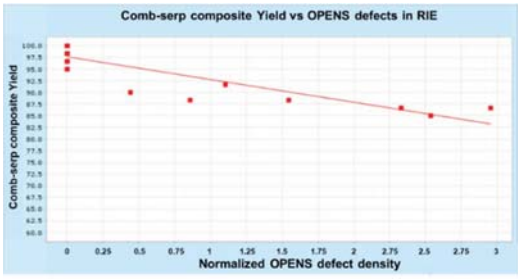


Fig. 4 In-line electrical yield of the large comb-serp macro against line open defects of post RIE.

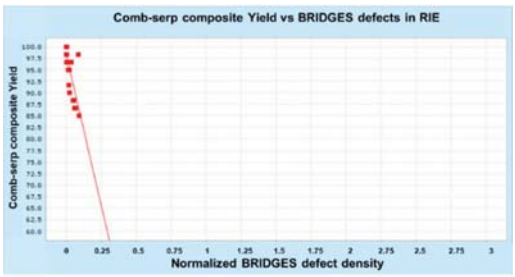
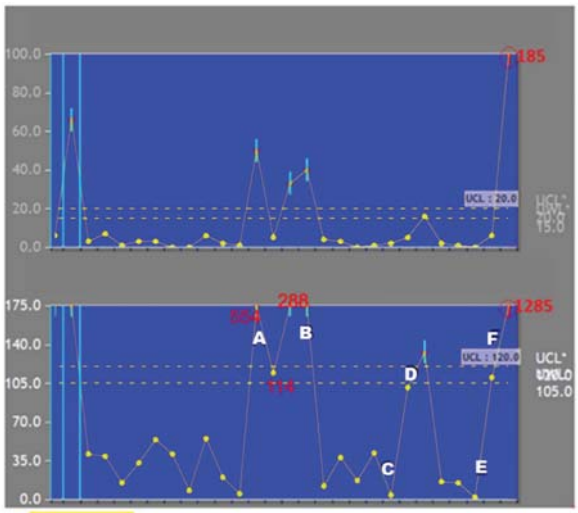


Fig. 5 In-line electrical yield of the large comb-serp macro against line bridge defects of post RIE.



A POR Wafers
B POR Wafers
C Blanket wafers post dielectric depostion
D POR wafers
E POR wafers
F Blanket wafers post dielectric etch + clean

Fig. 6 Particle count in the degas chamber of a PVD barrier seed deposition system after running several kinds of wafers.

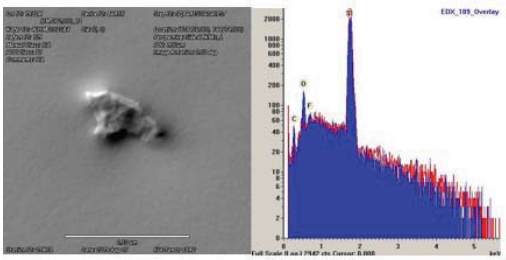


Fig. 7 SEM image of particles found in wafers that failed particle count in the degas chamber. EDX shows C-F signal.

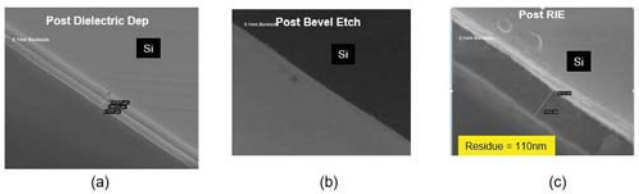


Fig. 8 Bevel cut after (a) Dielectric Deposition (b) Bevel Etch (c) Dielectric Etch

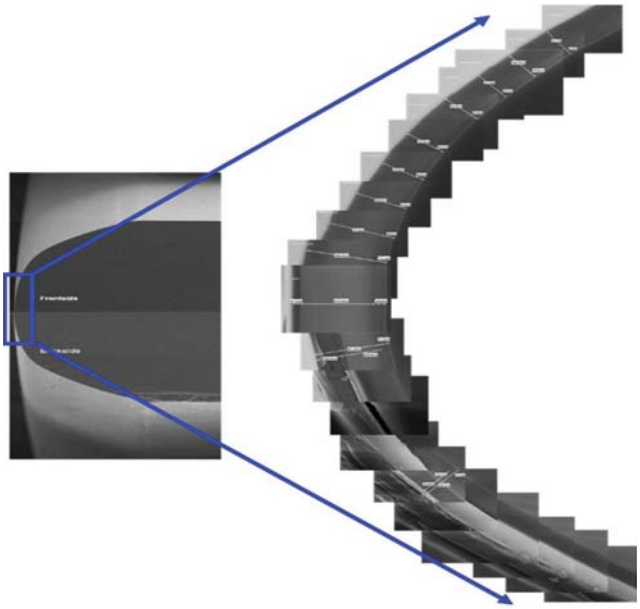


Fig. 9 SEM micrographs around the bevel confirms the RIE residue extended to 0.1-0.2 mm of the backside.

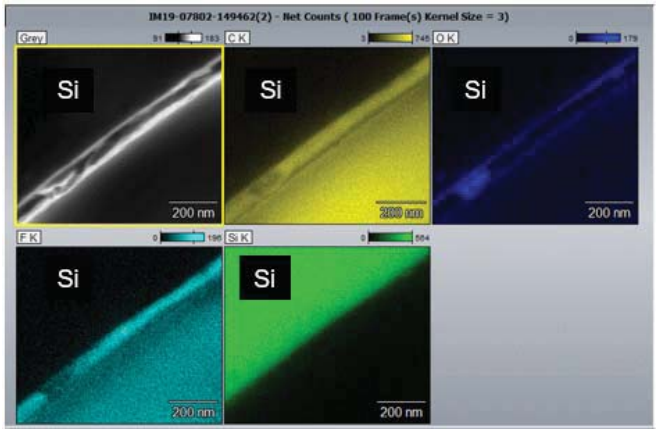


Fig. 10 EDX elementary mapping at 0.1 mm wafer backside. It is showing fluorine polymer on the surface.

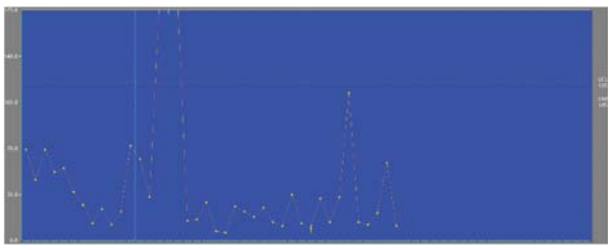


Fig. 11 Particle count in the degas chamber has stabilized after introduction of PET and purge in the degas chamber.

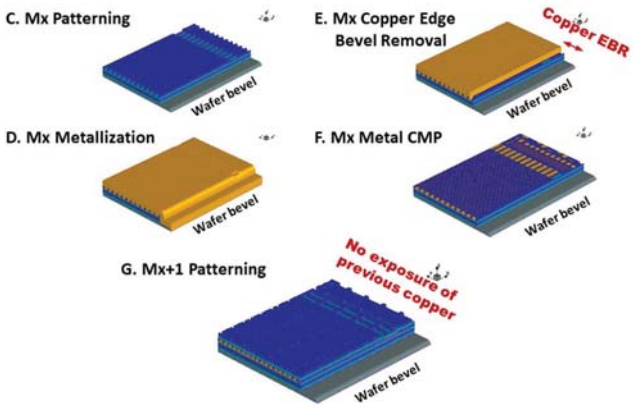


Fig. 12 Process emulation showing the major process steps in Bevel etch and copper EBR in this study.

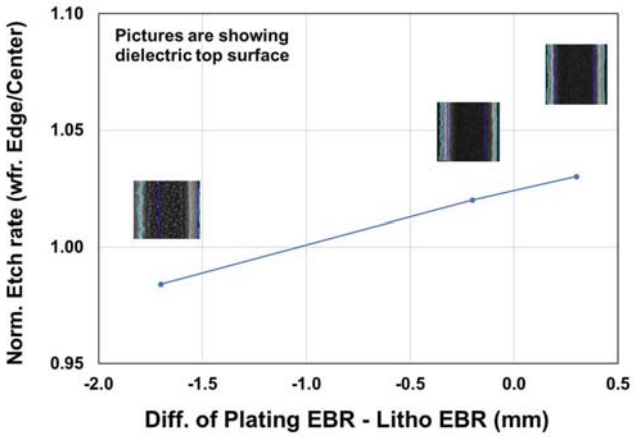


Fig. 13 Impact of edge copper ring to dielectric etch rate. The more minus number in the X-axis is indicating wider edge copper ring. The width of copper ring decreases the etch rate linearly.

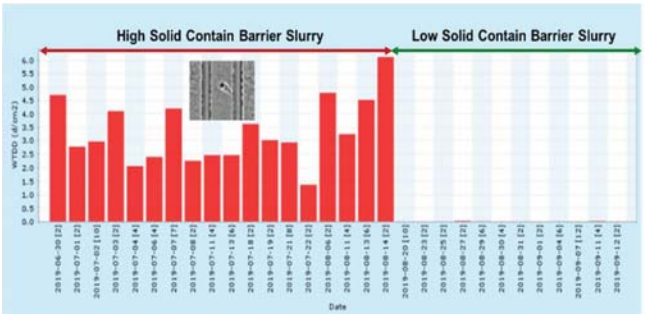


Fig. 14 The defectivity trend chart is showing the polishing scratches with high solid content (11.5 %) slurry versus a low solid content (2 %) slurry. The low solid content slurry reduces the scratches significantly.